migrates the source layout 110 to a migrated layout 150 which is more compact and which complies with the inputted rules and constraints.--.

Please enter the following replacement paragraph for the single full paragraph on page 19:

--The gate-expansion sub-arrangement implements gate expansion operations with respect to the FIG. 15 gate expansion treatment block 1510. As non-exhaustive examples, gate expansion candidates and/or gate expansion size may be automatically determined taking into consideration: the old design rules used to design the original source layout; the user-specified constraints 140 (as indicated by the FIG. 2 dashed arrow 290); the target process design rules 130 being used to design (i.e., compact) the layout (as indicated by the FIG. 2 dashed arrow 280); or, any combination thereof. The automatic re-legging arrangement 260 may also, or alternatively, allow a user to stipulate gate expansion candidates and/or gate expansion size. As further example embodiments, gate expansion may be globally applied for all transistor re-legging candidates, or only selectively applied for a lesser number of the transistor re-legging candidates. As a final note, care must be taken with gate expansion so as not to overlap neighboring layout structures so as to maintain proper electrical isolation (i.e., avoid short-circuiting in the final migrated layout). With the foregoing in mind, FIG. 9 illustrates a gate-expanded layout where all three of the transistor re-legging candidates have expanded gate areas, i.e., T_{VE}, T_{YE}, T_{ZE}, whereas the other transistor areas T_W, T_X do not. Note the difference in the size of the gates aimed at re-legging and those that are not.--.

Please enter the following replacement paragraph for the paragraph spanning pages 24-26:

--Discussion turns next to trimming of poly under the slots and also contact preparations. More particularly, once slots are defined by the above procedures, they are mathematically or arithmetically subtracted from the poly-silicon layer. Thus, an original normal leg is turned into a plurality of (e.g., three) thin legs connected in parallel. Trimming the poly-silicon leaves two uncovered diffusions between adjacent legs which is in the source node (and drain node) of two legs connected together. Assume that the source node is left as uncovered diffusion. It then must be connected to the right side of the original leg. In a similar way, the right uncovered diffusion, which is now the drain node, must be connected to the left side of the original leg. In order to ease this task, seeds of contacts covered by metal pads are implanted in the uncovered diffusion area. FIG. 12 shows an enlarged view with respect to trimming and contact placement/sizing of the FIG. 10 slots T_{YS1}, T_{YS2}. Of particular interest, note that while the two FIG. 12 slots have been illustrated unequally trimmed in length, i.e., a FIG. 12 left-hand contact C is shorter in length that a right-hand contact. A reason for this (similar to the reason as in FIG. 4) is to avoid potential electrical interference (e.g., short-circuiting) between the re-legging contact seeds and a closely neighboring layout structure LS (e.g., a metal M1 edge). FIG. 13 illustrates a non-enlarged re-legged layout 1300 where trimming has been completed and a pair of contacts has been placed with respect to each of the aforementioned three transistor re-legging candidates. Finally, FIG. 14 show an enlarged view of only an upper portion of the FIG. 10 slots T_{ZS1}, T_{ZS2}, for the purpose of showing that, upon subtraction of the slot's extend area SE from the poly-silicon